**Name: -** Rishitha Rao

**ID NO: -** 21EL010

**Division: -** 04

**Year: -** 2023-24

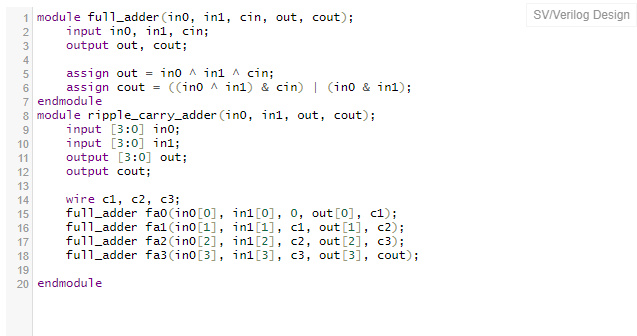
**Subject: -** Digital System Design (3EL42)

**Branch: -** Electronics

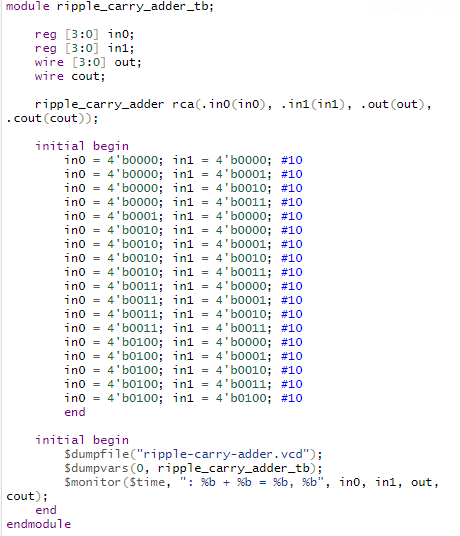
**Assignment 2**

**Q-1 Design 4-bit Ripple Carry Adder with the help of 1-bit adder.**

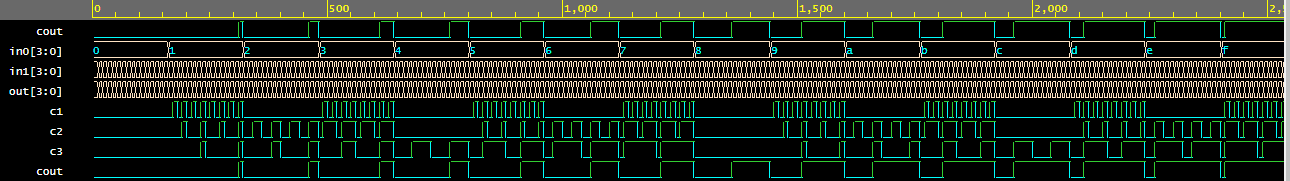
VERILOG CODE:-



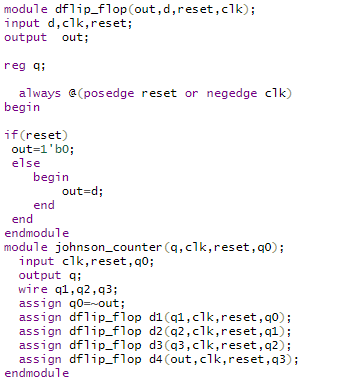
TEST BENCH:-



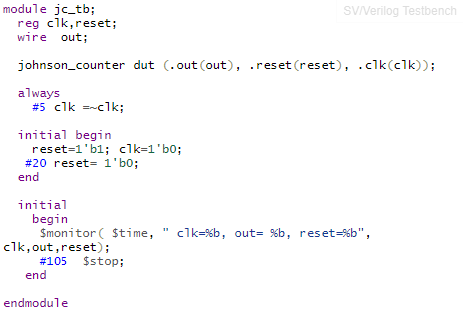
OUTPUT: -



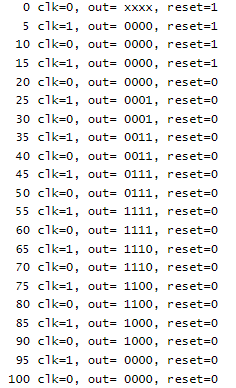
**Q-2 Design D-flipflop and reuse it to implement 4- bit Johnson Counter.**



TEST BENCH:-

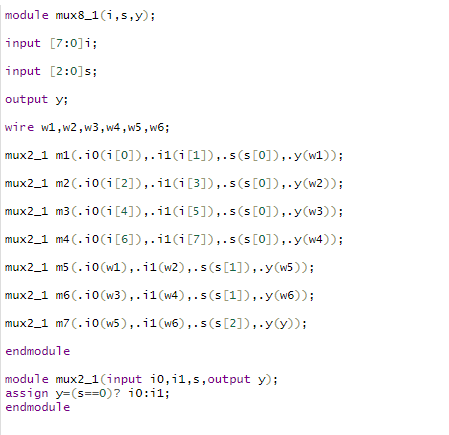


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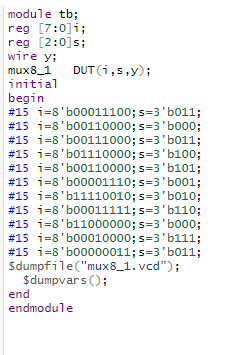


**Q-3 Reuse 2:1 Mux code to implement 8:1 Mux.**

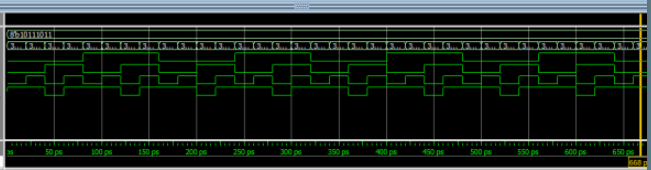
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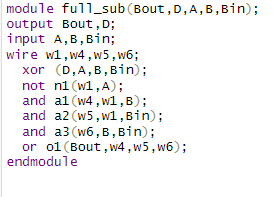


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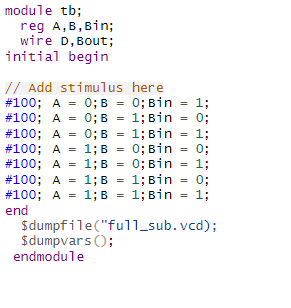


**Q-4 Design a Full Subtractor with Gate Level Modelling Style (Use primitive gates).**

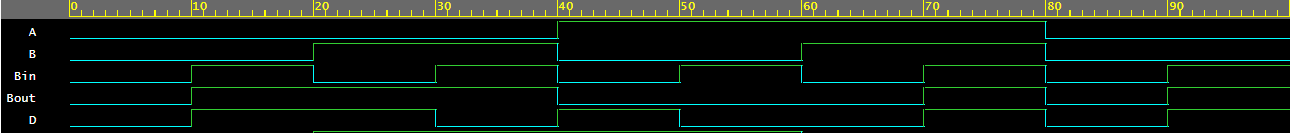
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TEST BENCH:-

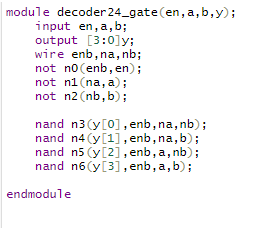


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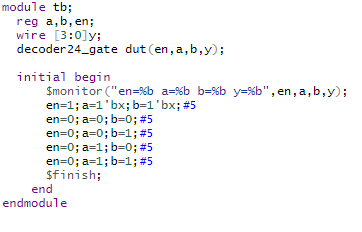


**Q-5 Design a 2X4 decoder using gate level modelling.**

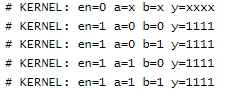
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TEST BENCH:-

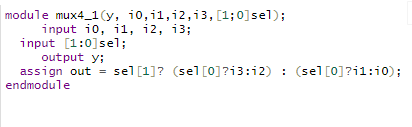


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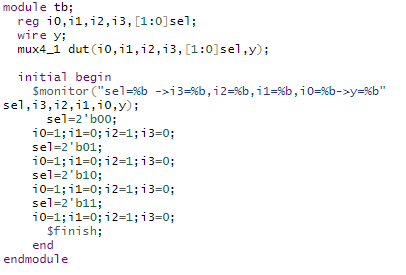


**Q-6 Design a 4x1 mux using operators. (Use data flow)**

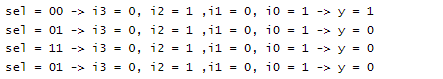
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TEST BENCH: -

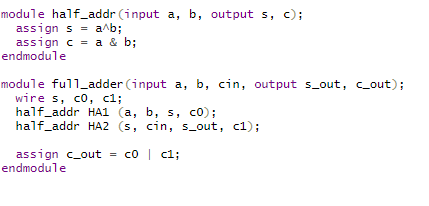


OUTPUT: -

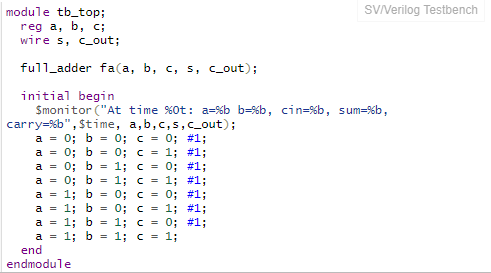


**Q-7 Design a Full adder using half adder.**

VERILOG CODE:-



TEST BENCH: -



OUTPUT: -

